AMENDMENTS to the CLAIMS

1. (Twice Amended) A method of transmitting digital information, comprising the steps of:

(a) transmitting a first word of a packet, comprising the steps of:

(1) transmitting start information onto a [first] bus, wherein the start information indicates a start of the packet;

(2) transmitting lower order memory address bits onto a [first] group of [second] bus lines of the bus; and

(3) transmitting first op_code information onto [an Nth] a first bus line of the [second] bus [lines, wherein N is an integer, and] wherein the [Nth] first bus line is not a bus line within the [first] group of [the second] bus lines; and

(b) transmitting a second word of the packet, comprising the steps of:

(1) transmitting second op code information onto the [first] bus;

(2) transmitting higher order memory address bits onto the [first] group of [the second] bus lines; and

(3) transmitting third op code information onto the [Nth] first bus line [of the second bus lines].

2. The method of claim 1 of transmitting digital information, further comprising the steps of:

(a) transmitting a third word of [a] the packet, comprising the steps of:

(1) transmitting a master device code for detecting collisions;

(2) transmitting count information for determining a count of a number of bytes of a memory transaction.

3. (Thrice Amended) In a digital system comprising a master device and at least one memory device, a process for transmitting memory requests to the memory device comprising the steps of:

transmitting a first word of a packet, comprising the steps of:

transmitting start information onto a [first] bus [line], said start information indicating the start of the packet[,];

transmitting a first portion of a lower order memory address bits onto a [first] group of [second] bus lines of the bus, said lower order memory bits comprising information to perform page mode memory accesses[,]; and

transmitting a first portion of op code information onto [a second group] at least a first bus line of the [second] group of bus lines; and

transmitting a second word of the packet, comprising the steps of:

transmitting a second portion of op code information onto the first bus line[,];

transmitting a third portion of op code information onto the at least a first bus line [second group] of the [second] group of bus lines, wherein an op code for page mode accesses can be detected from said first, second and third portions of op code information; and

transmitting a second portion of the lower order memory address bits onto the [first] group of [the second] bus lines;

wherein page mode access can be performed after transmission of the second word of the packet.

4. In a computer system comprising a master device and at least one memory device, a bus system for transmitting memory requests to the memory device comprising:

a plurality of bus lines for transmission of memory requests;

a packet comprising a memory request for transmission across the plurality of bus lines, said packet comprising:

a first word comprising:

start information indicating the start of the packet;

a first portion of lower order memory address bits comprising information to perform page mode memory accesses; and

a first portion of op code information; and

a second word comprising:

a second and a third portion of op code information, wherein an op code for page mode accesses can be detected from the first, second and third portions of op code information, and

a second portion of [the] lower order memory address bits;

wherein page mode access can be performed after transmission of the second word of the packet.

5. The bus system as set forth in claim 4 wherein said start information is located at a predetermined location in the first word of the packet, said system further comprising:

means for monitoring [the] a predetermined location in each word of the packet during transmission of [subsequent] the words of the packet that are subsequent to the first and second words for information other than the start information [of the packet]; and

means for detecting a collision if information occurs at the predetermined location in [subsequent] words of the packet that are subsequent to the first and second words, said information occurring due to [the] start information of another [a second] packet overlapping the [first] packet.

6. The bus system as forth in claim 5, wherein said packet further comprises a code identifying [the] a device transmitting the packet, said means for detecting a collision further comprising means for detecting the code to determine whether [where] the code is valid, an invalid code resulting from a collision between the packet and another packet [of packets].

7. The bus system as set forth in claim 4, wherein said packet further comprises count information indicating the number of bytes of [memory] data to be transmitted across the bus lines during [the] a [memory] transaction corresponding to the memory request [requested].

8. The bus system as set forth in claim 7, wherein said data is transmitted in a plurality of multiple byte blocks [block format], said system further comprising:

means for generating a first mask for data in a [the] first multiple byte block of the plurality of multiple byte blocks [data to be transmitted], said first mask indicating [the] which bytes of the first multiple byte block [which] are part of the transaction [memory operation requested]; and

means for generating a second mask for data in a [the] last multiple byte block of the plurality of multiple byte blocks, said second mask indicating [the] which bytes of the last multiple byte block [which] are part of the transaction [memory operation requested].

9. The bus system as set forth in claim 8, wherein each multiple byte block of the plurality of multiple byte blocks [data] is transmitted in 4 byte blocks, the first mask is generated from [the] two least significant bits of the lower order memory address bits and the second mask is generated from [the] two least significant bits of the count information.

10. The bus system as set forth in claim 8, further comprising a first and second look up table each comprising mask patterns, said first and second masks being generated by performing a table lookup of the first and second look up tables respectively using the address bits and the count information.

11. The bus system as set forth in claim 4, further comprising a summing means for summing [the] two least significant address bits and an internal byte count to produce [an] overflow information [value] and count information, said overflow information indicating [that although [the size] an amount of [the] data corresponding to [of] the memory request is less than the maximum number of bytes allowed in [the] a memory operation corresponding to the memory request, [the] granularity of [the] a multiple byte block format transmitted across [acres] the plurality of bus lines prohibits [the] a transaction, and, the memory request [should be] is separated into two separate memory requests.

12. A method of operation in a memory device, the memory device having an array of memory cells, the method comprising:

receiving first operation code information during a first clock cycle of an external clock signal;

receiving second operation code information successively after receiving the first operation code information;

receiving a first column address, the first column address representing a column locality of a first storage location within a first row in the array;

receiving a first row address successively after receiving the first column address, the first row address representing a location of the first row in the array; and

accessing a first memory cell of the array of memory cells, the first memory cell being located at the first storage location, wherein data stored in the first memory cell is accessed for a memory operation based at least in part on the first and second operation code information.

13. The method of claim 12 further comprising:

receiving a second column address and page mode control information, the second column address representing a column locality of a second storage location within the first row in the array; and

accessing a second memory cell of the array of memory cells, the second memory cell being located at the second storage location.

14. The method of claim 13 further comprising receiving a second row address in succession to receiving the second column address, the second row address representing the location of the first row in the array.

15. The method of claim 13 wherein the first column address and the first row address are both included in a first packet, and the second column address and the page mode information are included in a second packet.

16. The method of claim 12 wherein the first column address is received in a first portion of a packet and the first row address is received in a second portion of the packet.

17. The method of claim 16 wherein the packet further includes start information representing the beginning of the packet.

18. The method of claim 12 further comprising receiving block size information, the block size information representing an amount of data to be output by the memory device.

19. The method of claim 12 wherein the first column address is received during the first clock cycle and the first row address is received during a second clock cycle.

20. The method of claim 19 wherein a first portion of the first column address is received during a first bus cycle and a second portion of the first column address is received during a second bus cycle, and wherein both the first and second bus cycles transpire during the first clock cycle.

21. The method of claim 12 further comprising receiving page mode access information.

22. The method of claim 21 wherein the page mode access information is received concurrently with the first column address.

23. The method of claim 21 wherein the page mode access information includes a code wherein:
in a first state of the code, the memory device is operable in a page mode; and
in a second state of the code, the memory device is operable in a normal mode.

24. The method of claim 21 wherein the page mode access information includes a first portion and a second portion, wherein the first portion is received concurrently with the first column address, and the second portion is received concurrently with the first row address.

25. The method of claim 24 wherein the first portion of the page mode access information and the first column address are both included in a first portion of a packet, and wherein the second portion of the page mode access information and the first row address are both included in a second portion of the packet.

26. A method of controlling a memory device, the memory device having an array of memory cells, the method comprising:
issuing first operation code information during a first clock cycle of an external clock signal;
issuing second operation code information following the issuance of the first operation code information;

issuing a first column address to the memory device, the first column address representing a column locality of a first storage location within a first row in the array; and

issuing a first row address following the issuance of the first column address, the first row address representing a location of the first row in the array, wherein data stored in a memory cell located at the location is accessed for a memory operation based at least in part on the first and second operation code information.

27. The method of claim 26 further comprising issuing a second column address and page mode control information, the second column address representing a column locality of a second storage location within the first row in the array.

28. The method of claim 27 further comprising issuing a second row address following the issuance of the second column address, the second row address representing the location of the first row in the array.

29. The method of claim 28 wherein the first column address and the first row address are both included in a first packet, and the second column address and the page mode information are included in a second packet.

30. The method of claim 26 wherein the first column address is issued in a first portion of a packet and the first row address is issued in a second portion of the packet.

31. The method of claim 30 wherein the packet further includes start information representing the beginning of the packet.

32. The method of claim 26 further comprising providing block size information, the block size information representing an amount of data to be output by the memory device.

33. The method of claim 32 wherein the first column address, the first row address and the block size information are included in a packet.

34. The method of claim 33 wherein the first column address, the first row address and the block size information are included in the same packet.

35. The method of claim 26 wherein the first column address is issued during the first clock cycle, and the first row address is issued during a second clock cycle.

36. The method of claim 35 wherein a first portion of the first column address is issued during a first bus cycle and a second portion of the first column address is issued during a second bus cycle, and wherein both the first and second bus cycles transpire during the first clock cycle.

37. The method of claim 26 further comprising providing page mode access information.

38. The method of claim 37 wherein the page mode access information is provided concurrently with the issuance of the first column address.

39. The method of claim 37 wherein the page mode access information includes a code wherein:

when the code is in a first state, the memory device operates in a page mode; and

when the code is in a second state, the memory device operates in a normal mode.

40. The method of claim 37 wherein the page mode access information includes a first portion and a second portion, wherein the first portion is provided concurrently with the issuance of the first column address, and the second portion is provided concurrently with the issuance of the first row address.

41. The method of claim 40 wherein the first portion of the page mode access information and the first column address are both included in a first word of a packet, and wherein the second portion of the page mode access information and the first row address are both included in a second word of a packet.